REMARKS

This application has been reviewed in light of the Office Action dated November 27, 2006. Claims 1-32 are pending in the application. By the present amendment, claims 1, 11, 13, 21, 23, 30, 32 have been amended. No new matter has been added. The Examiner's reconsideration of the rejection in view of the amendment and the following remarks is respectfully requested.

By the Office Action, the Examiner objected to claims 11, 21, and 30 due to informalities. The current status of these claims is reflected in the claims listing above. Claims 11, 21, and 30 are currently amended from their unentered amendment form. Reconsideration is earnestly solicited.

By the Office Action, claims 1-32 stand rejected under 35 U.S.C. §102 (e) as being anticipated by U.S. Patent No. 6,629,292 to Corson et al. (hereinafter Corson).

Corson is directly to a system and method for applying an image to a semiconductor substrate. A semiconductor substrate is a fabricated semiconductor material. On the surface thereof lines are placed in order to render an image. Simply stated, Corson is drawing a picture on a substrate by using line segments of different densities to provide the details of the image.

Corson includes applying a gray scale image onto a surface of a semiconductor substrate in segments where the width of a line varies with gray scale level. Corson is completely different from the present claims and fails to anticipate the present invention. Corson starts with an image and adapts the image to be rendered on a chip (to draw a picture on the chip).

In stark contrast, the present invention begins with an integrated circuit chip design and then converts this design into a two-dimensional map. The pixels in the map represent properties of a corresponding area or a composite of layers for the corresponding location in the design. Each pixel is colored according to the magnitude of a property being analyzed. This provides a pixel map or a visual image representing the properties of the pixels across the map (e.g., metal fraction, heat load, etc.). The chip design is transformed to an easily analyzable image for that design depicting a given property. The present claims are completely different from the cited reference.

Claim 1 includes, *inter alia*, a method for analyzing circuit designs, including ... discretizing a design representation into displayable pixel elements representative of a structure in the design where each pixel element represents a portion of the design where the portion represents a geometric feature; determining at least one property for each pixel element representing the portion of the design where the at least one property is represented by an intensity of the pixel element, such that the pixel elements provide a pixel map to visually represent the design representation based on the at least one property; and determining a response of the design due to local properties across the design based upon representations of the pixel elements.

By the present claims, a design representation is discretized into displayable pixel elements representative of a structure in the design where each pixel element represents a portion of the design where the portion includes a geometric feature. In one example, a computer aided design image is broken up into pieces, each piece or portion is represented by a pixel. Then, for a given property (say e.g., metal fraction) each pixel is represented by an intensity. So that if,

e.g., the pixel had high metal fraction the pixel would be darker and low metal fraction the pixel would be lighter. The intensity represents the level or magnitude of the property for the corresponding location in the circuit design that the pixel represents. Then, a response is determined for the design due to local properties across the design based upon representations of the pixel elements. This gives an easy and fast way to reduce a circuit design to a visual representation so that design decisions can be made on the design, e.g., before manufacturing the design.

Corson fails to disclose or suggest any of these elements. Corson provides "pixel elements" (e.g., areas of reflectivity, col. 4, lines 54-55) by manufacturing a semiconductor device to have reflective or non-reflective surfaces. The so-called pixels are actually formed structures on the surface of a semiconductor device. In addition, line segments and other structures have their density and size controlled by lithography to render an image on a manufactured device. This is completely different from the claimed invention

Corson does not discretize a design representation into displayable pixel elements which represent a structure in the design. The pixels in Corson are the actual structure itself (e.g., metal lines, etc.) and these structures actually reflect light to help produce the effect of an image when the actual device is viewed. Corson does not have pixel elements that represent a portion of the design where the portion represents a geometric feature. The pixel element in Corson represents a portion of an image not a portion of a circuit design. This is completely different.

Corson does not determine at least one property for each pixel element representing the portion of the design where the at least one property is represented by an

intensity of the pixel element, such that the pixel elements provide a pixel map to visually represent the design representation based on the at least one property. Corson does the opposite. That is, Corson represents an image by creating a structure on a manufactured semiconductor device, not representing a property of a circuit design using a pixel's intensity.

Nowhere in Corson is determining a response of the design due to local properties across the design based upon representations of the pixel elements disclosed or suggested. It is therefore respectfully submitted that Corson fails to disclose or suggest the present claims.

The concepts and recitation of elements of the present claims are not even suggested by Corson. For example, Corson does not determine a response of the design due to local properties across the design based upon representations of the pixel elements. Similar reasoning is applicable to claims 13, 23 and 32. Claims 1, 13, 23 and 32 are therefore believed to be in condition for allowance for at least the reasons stated. Claims 2-12, 14-22 and 24-31 are also believed to be in condition for at least the stated reasons and due to their dependencies from claims 1, 13 and 23, respectively. The dependent claims include many features and elements also not disclosed or suggested by Corson. Early and favorable consideration is earnestly solicited.

In view of the foregoing amendments and remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

It is believed that no additional fees or charges are currently due. However, in the event that any additional fees or charges are required at this time in connection with the application, they may be charged to applicant's IBM Deposit Account No. 50-0510.

Respectfully submitted,

Date: 2/26/07

By: _____
James J. Bitetto
Registration No. 40,513

Mailing Address:
KEUSEY, TUTUNJIAN & BITETTO, P.C.
20 Crossways Park North, Suite 210
Woodbury, NY 11797
Tel: (516) 496-3868 Fax: (516) 496-3869